

CLAIMS

1. Test circuitry for testing an integrated circuit, the integrated circuit being configurable to accept input data from stimulus scan cells and to provide output data to response scan cells, the test circuitry including:

stimulus circuitry for providing test data to the integrated circuit;

input selection means operable to control which of the test data and the input data are received at the integrated circuit;

- capture circuitry for capturing output data from the integrated circuit and generating response data;

output selection means operable to select which of the output data and the response data are received by the response scan cells.

2. Test circuitry according to claim 1, wherein the input selection means includes a first multiplexor, the first multiplexor accepting the input data and the test data as inputs and outputting to the test circuitry.

3. Test circuitry according to claim 1, wherein the output selection means includes a second multiplexor, the second multiplexor selectively accepting the output data and the response data as inputs and outputting to the response scan cells.

4. Test circuitry according to claim 1, wherein the input selection means includes a first demultiplexor, the first demultiplexor accepting the input data as input and selectively outputting to either the stimulus circuitry or the integrated circuit.

5. Test circuitry according to claim 1, wherein the output selection means includes a second demultiplexor, the second demultiplexor accepting the output data as input and selectively outputting to either the capture circuitry or the response scan cells.

6. Test circuitry according to claim 1, configured to receive clock pulses from a clock generator, such that data is clocked into the scan cells with each received clock pulse.

5 7. Test circuitry according to claim 1, configured for selective operation in a test mode and an operative mode, wherein:

(a) in the test mode:

the stimulus circuitry is configured to receive the input data from the stimulus scan cells;

10 the input selection means is configured such that the integrated circuit receives the test data; and

the output selection means is configured such that the response scan cells receive the response data; and

(b) in the operative mode:

15 the input selection means is configured such that the integrated circuit receives the input data; and

the output selection means is configured such that the response scan cells receive the output data.

20 8. Test circuitry according to claim 7, wherein, in the test mode, the stimulus circuitry and the capture circuitry receive clock signals from a clock generator, the stimulus circuitry responding to the clock signals by writing the test data into the memory block when a memory write is enabled, and the capture circuitry responding to the clock signals by reading the response data from the memory block when a memory
25 read is enabled.

9. Test circuitry according to claim 1, wherein the stimulus circuitry includes:

a dictionary storing a plurality of read/write operation primitives, the primitives being combinable to form at least a first read/write testing sequence;

an address generator for generating addresses to which the primitives are written; and

a librarian sub-block for receiving the input data, the input data being indicative of a test to be applied to the integrated circuit, the librarian sub-block being configured to control, on the basis of the input data, which of the primitives are provided to the integrated circuit, and the order in which they are provided, based on the input data.

10. Test circuitry according to claim 1, wherein the integrated circuit is a memory circuit.

11. Test circuitry for testing an integrated circuit, the test circuitry including stimulus circuitry and capture circuitry, the stimulus circuitry including:

a dictionary storing a plurality of read/write operation primitives, the primitives being combinable to form at least a first read/write testing sequence; and

a librarian sub-block for receiving the input data, the input data being indicative of a test to be applied to the integrated circuit, the librarian sub-block being configured to control, on the basis of the input data, which of the primitives are provided to the integrated circuit, and the order in which they are provided, based on the input data;

wherein the capture circuitry captures response data from the integrated circuit

12. Test circuitry according to claim 11, wherein the integrated circuit includes a plurality of data addresses upon which the read/write operations are performed, the stimulus circuitry further including an address generator for generating addresses to which the primitives are written.

13. A method of testing an integrated circuit using test circuitry associated therewith, the test circuitry including:

stimulus circuitry;

input selection means;

capture circuitry; and

output selection means;

the integrated circuit being configurable to accept input data from stimulus scan cells and to provide output data to response scan cells, the method including the steps
5 of:

providing test data to the integrated circuit from the stimulus circuitry;

operating the input selection means to control which of the test data and the input data are received at the integrated circuit;

capturing output data from the integrated circuit using the capture circuitry;

10 generating response data based on the output data;

operating the output selection means to select which of the output data and the response data are received by the response scan cells.

14. A method according to claim 13, wherein the input selection means includes a first multiplexor, the first multiplexor accepting the input data and the test data as inputs
15 and outputting to the test circuitry.

15. A method according to claim 13, wherein the output selection means includes a second multiplexor, the second multiplexor selectively accepting the output data and the response data as inputs and outputting to the response scan cells.
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16. A method according to claim 13, wherein the input selection means includes a first demultiplexor, the first demultiplexor accepting the input data as input and selectively outputting to either the stimulus circuitry or the integrated circuit.
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17. A method according to claim 13, wherein the output selection means includes a second demultiplexor, the second demultiplexor accepting the output data as input and selectively outputting to either the capture circuitry or the response scan cells.

18. A method according to claim 13, the test circuitry being configured to receive clock pulses from a clock generator, such that data is clocked into the scan cells with each received clock pulse.

5 19. A method according to claim 13, wherein the test circuitry is configured for selective operation in a test mode and an operative mode, wherein:

(a) in the test mode:

the stimulus circuitry is configured to receive the input data from the stimulus scan cells;

10 the input selection means is configured such that the integrated circuit receives the test data; and

the output selection means is configured such that the response scan cells receive the response data; and

(b) in the operative mode:

15 the input selection means is configured such that the integrated circuit receives the input data; and

the output selection means is configured such that the response scan cells receive the output data.

20 20. A method according to claim 19, wherein, in the test mode, the stimulus circuitry and the capture circuitry receive clock signals from a clock generator, the stimulus circuitry responding to the clock signals by writing the test data into the memory block when a memory write is enabled, and the capture circuitry responding to the clock signals by reading the response data from the memory block when a memory read is
25 enabled.

21. A method according to claims 13, wherein the stimulus circuitry includes:

a dictionary storing a plurality of read/write operation primitives, the primitives being combinable to form at least a first read/write testing sequence;

an address generator for generating addresses to which the primitives are written; and

a librarian sub-block for receiving the input data, the input data being indicative of a test to be applied to the integrated circuit, the librarian sub-block being configured to control, on the basis of the input data, which of the primitives are provided to the integrated circuit, and the order in which they are provided, based on the input data.

22. A method according to claim 13, wherein the integrated circuit is a memory circuit.

23. A method for testing an integrated circuit using test circuitry, the test circuitry including stimulus circuitry and capture circuitry, the stimulus circuitry including:

a dictionary storing a plurality of read/write operation primitives, the primitives being combinable to form at least a first read/write testing sequence; and

a librarian sub-block;

the method including the steps of:

receiving input data at the librarian sub-block, the input data being indicative of a test to be applied to the integrated circuit;

selecting, on the basis of the input data and using the librarian sub-block, one or more of the primitives and an order of the primitives so selected;

providing the selected primitives to the integrated circuit in the selected order; and

capturing response data from the integrated circuit using the capture circuitry.

24. A method according to claim 23, wherein the integrated circuit includes a plurality of data addresses upon which the read/write operations are performed, the stimulus circuitry further including an address generator for generating addresses to which the primitives are written.

25. Test circuitry for testing an integrated circuit, the integrated circuit being configurable to accept input data from stimulus scan cells and to provide output data to response scan cells, the test circuitry including:

stimulus circuitry for providing test data to the integrated circuit;

5 input circuitry operable to control which of the test data and the input data are received at the integrated circuit;

capture circuitry for capturing output data from the integrated circuit and generating response data;

10 output circuitry operable to select which of the output data and the response data are received by the response scan cells.

1006307-020602